REMARKS

This is a full and timely response to the outstanding final Office Action mailed December 17, 2001. Reconsideration and allowance of the application and presently pending claims is respectfully requested.

Upon entry of this Response, claims 1-10, 17, 18 and 20 remain pending in this application. Claims 6 and 10 have been directly amended herein. It is believed that the foregoing amendments and additions add no new matter to the present application. Furthermore, the amendments to claim 6 merely place claim 6 in independent form by incorporating the limitations of pending claim 1 and, therefore, raise no new issues. In addition, claim 10 has been amended to specify that said wire-tracing level comprises a plurality of wire tracing levels. It is believed that claim 10, as amended, is allowable, and entry of the amendments to claims 6 and 10 is respectfully requested pursuant to 37 C.F.R. §1.116.

Claims 1-5, 17, 18 and 20 have again been rejected under 35 USC §103(a) as being unpatentable over Applicants' prior art FIG. 1 and FIG. 2. Claims 6-10 have again been rejected under 35 USC §103(a) as being unpatentable over Applicants prior art FIG. 1 and FIG. 2 in view of *Mizuno et. al.* (USP 6,140,686).

The Office Action acknowledges that prior art FIG. i and FIG. 2 of the present application fail to disclose, among other things, a first port that extends directly into a common area from a first area as required, by the claims 1 and 17 and all claims depending therefrom. However, the Office Action goes on to assert that it would have been obvious for the first port to extend directly from the first area into the common area, without the use of a linking area that includes bridge traces. The Office Action does not cite any reference or teaching that would support this assertion. In fact, neither FIG. 1 nor FIG. 2 of the present application suggest or otherwise teach such. On the off chance that there is room for a different view of what is taught or suggested by FIG. 1 and FIG. 2 of the present application, Applicants would respectfully request that such teaching or suggestion of a first port extending directly from the first area into the common area, without the use of a linking area that includes bridge traces, be specifically pointed out.

It is well settled law that in order to properly support an obviousness rejection under 35 U.S.C. §103, there must be some teaching in the prior art to suggest to one skilled in the art that the claimed invention would have been obvious. W.L. Gore &

Associates, Inc. v. Garlock Thomas, Inc., 721 F.2d 1540, 1551 (Fed. Cir. 1983). The Office Action herein has clearly failed to show any such teaching or suggestion.

The prior art has failed to recognize the problem to which the present invention is directed to solving. Recognition of a need, and the difficulties encountered by those skilled in the field, are classical indicia of unobviousness. In re Dow Chemical, 837 F.2d 469, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988).

The present invention recognizes the difficulties and needs imposed by the prior art and puts forth a solution to overcome these previously unrecognized difficulties and needs. As part of integrated circuit design, various methodologies are utilized in laying out the signal wiring that forms the signal paths that transfer signals from one block of circuitry to another. Because of inherent differences in the methodologies that are used in laying out the signal wiring, it is common for there to be resulting mismatches in port alignments. As a result, the ports on the various blocks of circuitry on an integrated circuit often do not precisely line up for easy and direct interconnection. Thus, efforts must be made to provide for an interface to link the different blocks of circuitry. Further, in order to combat degradation in signal quality due to long signal paths, it is common to buffer the signals with buffering circuitry in order to retain proper signal timing and amplitude. Buffering of signals has typically been carried out separately from providing for linking of mis-aligned ports as is illustrated in FIG. 1 and FIG. 2 of the present application. This has resulted in integrated circuit real estate being utilized for aligning mis-aligned ports separately from integrated circuit real estate used for providing for appropriate signal buffering. This has meant greater usage of integrated circuit real estate.

At this point, Applicants have to ponder the question of why, if it were really obvious to extend the first port directly from the first area into the common area as asserted by the Office Action, would sophisticated integrated circuit designers and manufacturers resort to the designs represented by the prior art of FIG. 1 and FIG. 2, when such designs waste so much valuable integrated circuit real estate? The answer is clear---the present claimed invention is simply not obvious. The present invention recognizes the previously unrecognized difficulties and needs imposed by the prior art and presents a solution. For at least these reasons, claims 1-10, 17, 18 and 20 are allowable as currently pending.

It is improper to use the benefit of hindsight analysis to declare an innovation obvious. Roberts v. Sears, Roebuck & Co., 723 F.2d 1324, 1334, 221 U.S.P.Q. 504 (7th Cir. 1984). Applicants respectfully submit that any notion of the obviousness of the invention specified by the claims 1-10, 17, 18 and 20 can be arrived at only by virtue of hindsight analysis, whereby the disclosure of the present invention is used as the template and elements from the prior art are used to fill the gaps. For at least this reason, Applicants submit that claims 1-10, 17, 18 and 20 are allowable as currently pending.

Claims 6-10 have again been rejected under 35 USC §103(a) as being unpatentable over the prior art FIG. 1 and FIG. 2 in the present application, in view of *Mizuno, et al.* (USP 6,140,686). With regard to claims 6 and 7, the Office Action again acknowledges that Applicants prior art FIG. 1 and FIG. 2 fail to disclose integrated circuit real estate comprising multi-levels. The Office Action asserts that *Mizuno, et al.* discloses an integrated circuit (FIG. 1, 21 and Abstract) comprising multi-levels wherein the multi-levels comprises a semiconductor level and a wiring level, the semiconductor level forms a buffer and control circuit so that the frequency of the oscillation output corresponds to the frequency of the clock signal (Abstract) and the wiring levels 110, 111, 112, 113 provide the power supply voltage to the circuit block 300 (FIG. 1). The Office Action asserts that it would have been obvious to one having ordinary skill in the art at the time of the invention to modify the integrated circuits of Applicants' prior art FIG. 1 and FIG. 2 so that the integrated circuit real estate comprises multi-levels to maintain the frequency of the signal from the clock to the oscillation output and provide the power supply voltage to the circuit block shown by *Mizuno, et al.*

Claim 6 has been amended herein as noted above to include all limitations of pending claim 1. Each and every limitation of claim 6, as amended herein, must be considered in determining the patentability of claims 6-10. The above discussions concerning the limitations of pending claims 1-5, 17, 18 and 20 are equally applicable to claims 6-10. In view of this, Applicants respectfully submit that independent claim 6, as amended herein, as well as claims 7-10, are allowable over the prior art. Reconsideration and allowance of these claims is respectfully requested.

The prior art of record does not teach or otherwise suggest an integrated circuit such as that specified by pending claims 1-10, 17, 18 and 20 herein. Applicants

respectfully submit that pending claims 1-5, 17, 18 and 20, as well as claims 6-10, are allowable over the prior art. Reconsideration and allowance of these claims is respectfully requested.

CONCLUSION

For at least the reasons set forth above, Applicants respectfully submit that pending claims 1-5, 17, 18 and 20, as well as amended claims 6-10, are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims is hereby respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 738-2378.

Respectfully submitted,

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ANNOTATED VERSION OF MODIFIED CLAIMS TO SHOW CHANGES MADE

The following is a marked up version of the amended claims, wherein bracketing denotes deletions and underlining denotes additions.

6. (Once Amended) [An integrated circuit according to claim 1 wherein] An integrated circuit comprising:

a first port located in a first area of integrated circuit real estate, for outputting a signal;

a second port located in a second area of integrated circuit real estate, for receiving said signal;

a common area comprising an alignment link for electrically connecting said first port with said second port;

said first port extends directly into said common area from a first area;

said second port extends directly into said common area from a second area;

said alignment link comprises a signal buffer for buffering a signal traveling along said alignment link between said first port and said second port; and

said integrated circuit real estate comprises multi-levels.

10. (Once Amended) An integrated circuit according to claim 9 wherein said wire-tracing level comprises a plurality of wire-tracing levels.